Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **A0**
2. **B0**
3. **O0**
4. **A1**
5. **B1**
6. **O1**
7. **GND**
8. **O3**
9. **B3**
10. **A3**
11. **O2**
12. **B2**
13. **A2**
14. **VCC**

**.047”**

**2 1 14 13 12**

**5 6 7 8 9**

**3**

**4**

**11**

**10**

**MASK**

**REF**

**.046”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .046” X .047” DATE: 3/17/17**

**MFG: FAIRCHILD THICKNESS .014” P/N: 54ACT32**

**DG 10.1.2**

#### Rev B, 7/1